IN THE CLAIMS:

Claim 1. (**Currently Amended**) An input/output interface, wherein

~~a~~ logical ~~value is~~ values are expressed respectively by ~~an order~~ orders that transition edges appear in a plurality of transmission signals transmitting respectively on a plurality of signal lines.

Claim 2. (**Currently Amended**) The input/output interface according to claim 1, wherein:

each of said transmission signals ~~include~~ includes a plurality of the transition edges; and

said logical ~~value is~~ values are expressed by combining the ~~order~~ orders that the respective transition edges appear in the transmission signals.

Claim 3. (**Currently Amended**) The input/output interface according to claim 2, wherein:

said transmission signals are pulse signals; and

said logical ~~value is~~ values are expressed by using the ~~order~~ orders that the transition edges appear in the pulse signals.

Claim 4. (**Currently Amended**) The input/output interface according to claim 3, wherein

said logical ~~value is~~ values are expressed by combining the ~~order~~ orders that leading edges appear in and the ~~order~~ orders that trailing edges appear in said pulse signals.

Claim 5. (**Original**) The input/output interface according to claim 4, wherein said plurality of the signal lines consists of three lines or more.

Claim 6. (**Original**) The input/output interface according to claim 1, wherein said transmission signals express one or both of data and an address.

Claim 7. (**Currently Amended**) The input/output interface according to claim 1, having a transmitting device for transmitting said transmission signals, the device comprising:

a transmitting circuit for selecting any of a plurality of timing signals for each of said signal lines according to said logical ~~value~~ values, the plurality of timing signals at transition edges having timings different from each other, and for generating each of said transmission signals in synchronization with each of the selected timing signals, respectively.

Claim 8. (**Currently Amended**) The input/output interface according to claim 7, wherein said transmitting circuit comprises:

a delay circuit including a plurality of delay stages connected in cascade, receiving a standard signal on an initial stage of the delay stages, and outputting each of said timing signals, which each is the standard signal delayed, from each delay stage;

a selecting circuit for selecting any one of the timing signals for each of said signal lines, according to the logical ~~value~~ values; and

an edge generator for generating the transition edge for each of said transmission signals, in synchronization with each of said selected timing signals.

Claim 9. (**Currently Amended**) The input/output interface according to claim 8, wherein:

said transmission signals are pulse signals;

said logical ~~value is~~ values are expressed by combining the ~~order~~ orders that leading edges appear and the ~~order~~ orders that trailing edges appear in ~~each of~~ said pulse signals;

said delay circuit outputs said timing signals for said leading edges and said trailing edges, respectively;

said selecting circuit includes a first selecting circuit and a second selecting circuit for the leading edge and the trailing edge, respectively; and

said edge generator generates the leading edges of said pulse signals in synchronization with said timing signals selected in said first selecting circuit, and the trailing edges of said pulse signals in synchronization with said timing signals selected in said second selecting circuit.

Claim 10. (**Original**) The input/output interface according to claim 9, wherein said edge generator includes an output transistor of an open drain type.

Claim 11. (**Currently Amended**) The input/output interface according to claim 8, wherein:

said transmitting circuit includes a decoder for decoding said logical ~~value~~ values; and

said selecting circuit selects the respective timing signals according to the result of the decoding by the decoder.

Claim 12. (**Currently Amended**) The input/output interface according to claim 1 having a receiving device for receiving said transmission signals, the device comprising:

a receiving circuit including a comparing circuit for comparing the ~~order~~ orders that the transition edges appear in said transmission signals, and a logical value generating circuit for generating the logical ~~value~~ values according to the result of the comparison by the comparing circuit.

Claim 13. (**Currently Amended**) The input/output interface according to claim 12, wherein

each of the logical ~~value~~ values generated by said receiving circuit is an original logical value used in a transmitting device for transmitting said transmission signals.

Claim 14. (**Currently Amended**) The input/output interface according to claim 12, wherein:

each of said transmission signals ~~include~~ includes a plurality of the transition edges; and

said comparing circuit includes a plurality of comparators for comparing the ~~order~~ orders that the respective transition edges appear in said transmission signals.

Claim 15. (**Original**) The input/output interface according to claim 14, wherein:

said transmission signals are pulse signals; and

said plurality of the comparators are a plurality of first comparators for comparing leading edges of said transmission signals and a plurality of second comparators for comparing trailing edges thereof.

Claim 16. (**Currently Amended**) The input/output interface according to claim 12, wherein:

said comparing circuit includes a plurality of flip-flops, each of which receives two different transmission signals of said transmission signals; and

said ~~order~~ orders that the transition edges appear ~~is~~ are decided according to output levels of the plurality of the flip-flops.

Claim 17. (**Currently Amended**) The input/output interface according to claim 12, wherein

said logical value generating circuit includes a decoder for decoding the result of the comparison and for generating said logical ~~value~~ values based on the result of the decoding.

Claim 18. (**Original**) The input/output interface according to claim 1, wherein

a transmitting circuit for transmitting said transmission signals and a receiving circuit for receiving said transmission signals are respectively formed on separate semiconductor chips.

Claim 19. (**Original**) The input/output interface according to claim 1, wherein

a transmitting circuit for transmitting said transmission signals and a receiving circuit for receiving said transmission signals are formed on the same semiconductor chip.

Claim 20. (**Original**) A semiconductor integrated circuit comprising a transmitting circuit, including:

a timing signal generator for generating a plurality of timing signals whose transition edges appear at different timings from each other;

a selecting circuit for selecting any of said timing signals for each plurality of signal lines, according to a logical value; and

an edge generator for generating transmission signals in synchronization with the selected timing signals, respectively, and for outputting the generated transmission signals.

Claim 21. (**Original**) A semiconductor integrated circuit comprising a receiving circuit, including:

a comparing circuit for comparing an order that transition edges appear in a plurality of transmission signals transmitting respectively through a plurality of signal lines; and

a logical value generating circuit for generating a logical value according to a result of the comparison by said comparing circuit.

Claim 22. (**Original**) An input/output interface, wherein

a logical value is expressed by a time difference between a transition edge of a transmission signal transmitting on a signal line and a transition edge of a standard timing signal.

Claim 23. (**Original**) The input/output interface according to claim 22, further comprising:

a transmitting circuit for converting the logical value, expressed with a plurality of bits, to a predetermined delay time, and for outputting said transmission signal, which is behind said standard timing signal by said delay time, to said signal line; and

a receiving circuit for detecting the delay time of the transition edge of said transmission signal transmitting through said signal line, to the transition edge of said standard timing signal, and for generating a logical value according to the detected delay time.

Claim 24. (**Original**) The input/output interface according to claim 23, wherein said transmitting circuit includes a variable delay circuit for delaying said standard timing signal according to said logical value to generate said transmission signal.

Claim 25. (**Original**) The input/output interface according to claim 23, wherein said receiving circuit comprises:

a delay circuit for generating a plurality of timing signals whose phases are different from that of said standard timing signal; and

a comparing circuit for comparing the phase of said transmission signal and the phases of said timing signals, respectively, and for detecting the delay time of said transmission signal with reference to said standard timing signal.

Claim 26. (**Original**) The input/output interface according to claim 25, wherein said comparing circuit comprises:

a plurality of latch circuits for latching logic levels of said transmission signal by said timing signals, respectively; and

an encoder for generating said logical value in accordance with the respective logic levels being latched in the latch circuits.

Claim 27. (**Original**) The input/output interface according to claim 23, wherein said transmission signal expresses one or both of data and an address.

Claim 28. (**Original**) The input/output interface according to claim 23, wherein said logical value generated by said receiving circuit is an original logical value used in the transmitting device for transmitting said transmission signal.

Claim 29. (**Original**) The input/output interface according to claim 23, wherein said transmitting circuit and said receiving circuit are respectively formed on separate semiconductor chips.

Claim 30. (**Original**) The input/output interface according to claim 23, wherein said transmitting circuit and said receiving circuit are respectively formed on the same semiconductor chip.

Claim 31. (**Original**) The input/output interface according to claim 23, wherein:

said transmitting circuit and said receiving circuit are respectively formed on a plurality of semiconductor chips; and

each of said semiconductor chips include a first input circuit and a second input circuit for respectively receiving a transmission signal and a standard timing signal which is outputted from another semiconductor chip, a signal generating circuit for generating another standard timing signal according to an external clock signal, and a first output circuit for outputting another transmission signal.

Claim 32. (**Original**) The input/output interface according to claim 31, wherein each of said semiconductor chips include a second output circuit for outputting said standard timing signal to the exterior of the respective chips.

Claim 33. (**Original**) The input/output interface according to claim 32, wherein an input of said second input circuit and an output of said second output circuit are connected to a common external terminal.

Claim 34. (**Original**) The input/output interface according to claim 31, wherein an input of said first input circuit and an output of said first output circuit are connected to a common external terminal.

Claim 35. (**Previously Presented**) A semiconductor integrated circuit comprising:

a transmitting circuit for converting a logical value to a predetermined delay time in accordance with the logical value, the logical value being expressed with a plurality of

bits, and for outputting a transmission signal, which is behind a standard timing signal by the delay time, to a signal line.

Claim 36. (**Previously Presented**) A semiconductor integrated circuit comprising a receiving circuit for receiving a transmission signal, which is behind a standard timing signal by a predetermined delay time in accordance to a logical value,

for detecting a delay time between a transition edge of the transmission signal transmitting through a signal line, and the transition edge of the standard timing signal, and

for generating the logical value according to the detected delay time.